

Summary

Claims 1-3 were pending. Claims 1 and 2 have been rewritten. No new matter has been added as a result of this amendment.

Claim Rejections

Claims 1 and 2 were rejected under 35 U.S.C. §102(b) as being anticipated by Iwasaki (U.S. Patent 5,513,222) and Claim 3 was rejected under 35 U.S.C. §103(a) as being unpatentable over Iwasaki in view of Hecken (U.S. Patent 4,373,207).

Claim 1 has been rewritten to recite that the diversity reception device includes receiver circuits, level comparator means, level variable means, and adder means.

The level comparator means includes first and second detector means and first and second comparator means. The first detector means detects a level of a signal output from the first receiver circuit while the second detector means detects a level of a signal output from the second receiver circuit. Each of the first and second comparator means compares the level of the signal detected by the first detector means with the level of the signal detected by the second detector means.

The level variable means interposed between the first receiver circuit and the adder means is controlled by a signal output from the first comparator means. The level variable means interposed between the second receiver circuit and the adder means is controlled by a signal output from the second comparator means. This permits each of the received signals, other than a received signal having a maximum level, to be relatively attenuated by the level variable means in accordance with the difference of the level of the received signal from the maximum level before being input into the adder means. Accordingly, the C/N ratio of a synthesized signal can be maximized without being influenced by variations in ambient conditions, such as temperature or power supply voltage.

Iwasaki does not anticipate or disclose such an arrangement. Iwasaki does not disclose comparator means as recited in Claim 1. To the contrary, Iwasaki discloses multiple weighing calculating circuits, each of which is connected solely to a different receiver circuit and thus is supplied with the signal from only one receiver

circuit. This is entirely unlike the arrangement of Claim 1 in which the levels of the signals from both of the first and second detector means (and thus both the first and second receiver circuits) are compared by each of the first and second comparator means.

Nor does Iwasaki disclose level variable means as recited in Claim 1. The level variable means of Iwasaki adjusts the level of a signal supplied thereto based on the signal from a single weighing calculating circuit and thus only on a signal from one receiver circuit. This is entirely unlike the arrangement of Claim 1 in which each level variable means adjusts the level of a signal supplied to the level variable means based on the signals from both receiver circuits.

For at least these reasons, Iwasaki does not anticipate or disclose the arrangement of Claim 1. Thus, Claim 1 is patentable over the cited references.

Claim 2 further recites that the phase shifter means is interposed between each of the first and second receiver circuits and the adder means. To the contrary, Iwasaki discloses a single phase shifter means, which is disposed between one of the receiver circuits and the adder means.

For at least this additional reason, Iwasaki does not anticipate or disclose the arrangement of Claim 2. Thus, Claim 2 is patentable over the cited references.

Conclusion

Applicants respectfully submit that all of the pending claims are in condition for allowance and seek an early allowance thereof. If for any reason the Examiner is unable to allow the application in the next Office Action and believes that a telephone interview would be helpful to resolve any remaining issues, she is respectfully requested to contact the undersigned.

Respectfully submitted,


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